Implementation of a High Rate Radio Receiver (HSP43124, HSP43168, HSP43216, HSP50110, HSP50210)

Features

• Modulation Formats: BPSK, QPSK, SQPSK, 8-PSK, FM, FSK

• Symbol Rates: To 22.5MSPS (4 Samples/Symbol)

• Programmable: Reconfigurable to Data Rate, Modulation Format, and Order/Type of Tracking Loop

• Digital: Repeatable Performance Over Temperature and Time

• High Performance Reception: Bit Error Rate Approaches Less Than 0.5dB From Theory

TABLE 1. INTERSIL DSP PRODUCTS FOR HIGH RATE DIGITAL RADIO RECEIVERS

| FUNCTIONAL BLOCK	INTERSIL PART
VCA	Analog Discrete
140MHz Quadrature Output 6-Bit A/D Converter (8-Bit A/D Converter)	HI3086JCQ, CXA3086Q (HI3026JCQ, HI3026AJCQ)
Decimating Filter	HSP43216 Halfband Filter
Digital DownConverter	HSP50110 Digital Quadrature Tuner
Matched Filter	HSP43168 Dual FIR Filter
Carrier and Symbol Tracking Loops	HSP50210 Digital Costas Loop
AGC Loop Filter	Analog Discrete
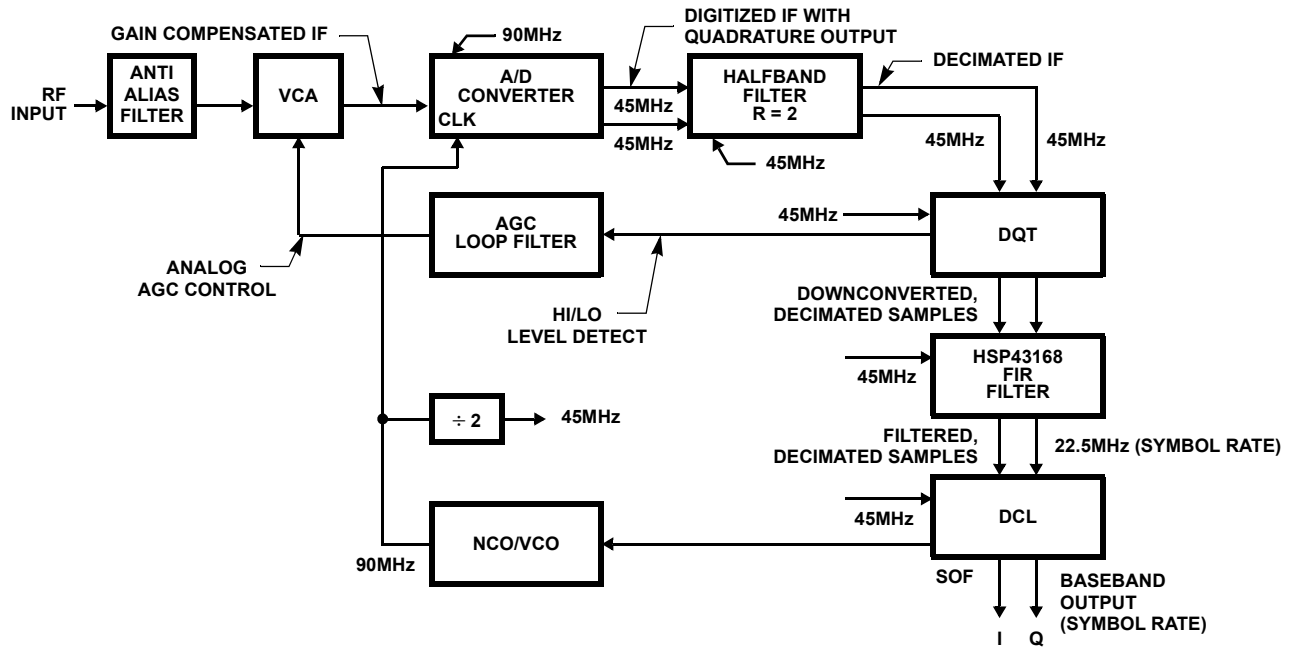
FIGURE 1. BLOCK DIAGRAM OF A HIGH RATE DIGITAL RADIO RECEIVER

Introduction

The present HSP50110/210EVAL Board provides capabilities for evaluating received modulated signals with symbol rates up to 2.5MSPS. This high end limit on symbol rate is based on 20 samples per symbol. Many applications do not require such a large number of samples per symbol, and can still use the HSP50110/210EVAL Evaluation Board to breadboard and test these applications. Two limitations come into play as higher rates are implemented with this Evaluation Board:

1. The Serial FIR Filter maximum clock rate is (45MHz/10 bits) = 4.5MHz.
2. The transport delay, or propagation delay in the loop causing loop instability for input rates above 4.5MHz.

It is these limitations that prompts the presentation of a high symbol rate receiver implementation using the HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chip set. Figure 1 illustrates a high rate receiver configuration using the DQT and DCL demod parts. This implementation will be offered as the design solution, after the design considerations and trades have been presented.

High Rate Design Concerns

The primary limitations on a high speed design are the maximum operating speed of the digital parts and the bandwidth and resolution on the A/D converter. These key parameters are listed for the parts that will be configured for our high rate receiver design.

Maximum Clock Speed of HSP43216:. 52MHz
Maximum Clock Speed of HSP50110:. 52MHz
Maximum Clock Speed of HSP43168:. 45MHz
Maximum Quadrature A/D
Conversion Speed:. . . . . 140MSPS with 6 Bits
120MSPS with 8 Bits
Minimum Number Samples
per Symbol . . . . 4 Samples/Symbol

Selecting An A/D Converter

The design begins with selecting a high speed, wide bandwidth, high resolution D/A converter. Devices exist that output dual demultiplexed data samples at half the sample rate. This relaxes the maximum clock rate of the following devices by 2. Such a device is the HI3086JCQ Intersil A/D. It is a 6-bit 140MSPS Flash A/D Converter with quadrature output samples. (The HI3026 A/D, an 8-bit 120MSPS device with dual demultiplexed output is also a design candidate). Subsequent DSP parts could operate up to a 70MHz maximum clock rate if the HI3086 is used.

Selecting The DSP Sample Rate

The Clock Rate Criterion

Selecting 4 samples per symbol yields the desired bandwidth. This sets the rate at which the HSP50110 Digital Quadrature Tuner will output symbol data. We can construct a DSP processing chain from this baseline symbol rate. The clock rate of the IF signal into the HSP50110 Digital

Quadrature Tuner is set to be four times the symbol rate. By using an HSP43216 Halfband Filter in the Downconvert and Decimate mode (INT/EXT# = 0), the dual channel demultiplexed sampled data from the A/D can be input at four times the symbol rate. By noting that the A/D outputs 2 synchronous samples at half the A/D sample clock rate, the A/D sample rate is effectively four times the symbol rate.

The Re-Sampler in the DQT eliminates the need for the sample clock and the symbol rate to be exact integer related. (An even integer is used as an example for clarity and to yield a "ball park" solution for applications with non integer relationships). Note that an external NCO is used to drive the A/D clock port. This minimizes the clocking jitter in the system. Use of the DQT Re-Sample NCO in addition to a separate clock generator for the A/D and halfband will inherently have more jitter than the configuration shown. The DQT is used in the complex input mode.

Determining the DSP System Limiting Rate

The next limiting clock DSP element is the Halfband Filter which has a maximum clock rate at 52MHz. The rate through this decimating filter part can be optimized by using it in the Downconvert and Decimate Mode (INT/EXT# = 0). This allows dual (demultiplexed) inputs at the maximum clock rate. This sets the maximum system sustainable clock rate at the output of the A/D converter at 52MHz per data stream. The maximum system sustainable A/D input sample clock becomes twice the A/D output clock, or 104MHz. The decimate by two HalfBand filter output becomes a quadrature data stream at 52MHz and the symbol rate is one half of this, or 26MHz (2 samples on I, 2 samples on Q = 4 samples per symbol).

System Design Considerations

Frequency Domain Considerations for the A/D Sample Rate

Determining the appropriate A/D sample rate, requires more than just consideration of the clocking criterion of the DSP parts. The frequency plan of the receive system must complement the digitizing hardware and not produce alias components that will impede the ability to recover the signal of interest. Thus it is equally important that the sample rate be selected in a location relative to the IF signal, in a way that will not cause alias signals to fall in band. Many applications use undersampling techniques to recover signals from IF carriers by locating a harmonic of the sample frequency at a strategic distance from the IF signal. An alias of the high frequency IF carrier is then processed by the DSP hardware.

Figure 2A and 2B illustrate two examples of how a 90MHz A/D sample clock can be used to downconvert and process modulated IF signals. Figure 2A shows an oversampled 20MHz IF, while Figure 2B shows an undersampled 160MHz IF.

Figure 3 illustrates the spectral development at several points in the data path in the Block Diagram, from IF input to baseband output. The example has $f_S' = f_S/2$ (Decimate by 2) in the HBF and $f_S'' = f_S'/8$ (Decimate by 8) in the DCL.
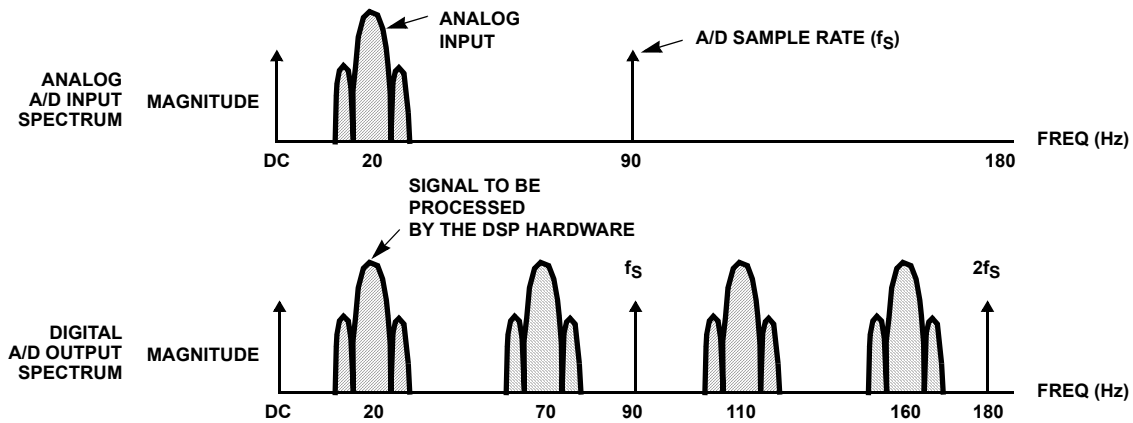
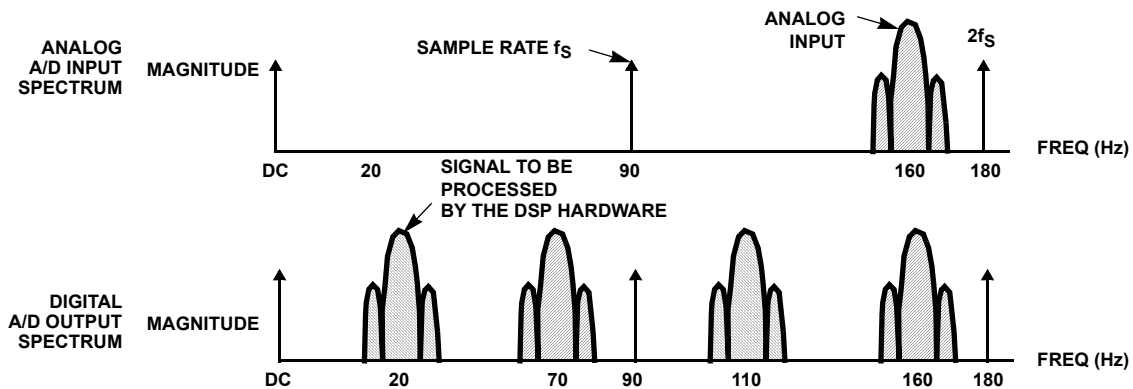FIGURE 2A. OVERSAMPLED 20MHz IF INPUT SPECTRAL PLOTS

FIGURE 2B. UNDERSAMPLED 120MHz IF INPUT SPECTRAL PLOTS

Additionally, it is insufficient to just consider the signals of interest. Those signals that fall in the band of the A/D converter must be removed by any anti-aliasing filters ahead of the A/D converter. These in band signals; if not filtered out, will also alias around the clock frequency and may appear directly on top of the signal of interest. In example B of Figure 2, a 70MHz signal will interfere in such a way. The anti alias filter should be designed to attenuate the undesired signals to the point that it prevents such signal degradation. Note that an important system trade is the implementation of the anti-alias filter and the selection of the A/D clock frequency.

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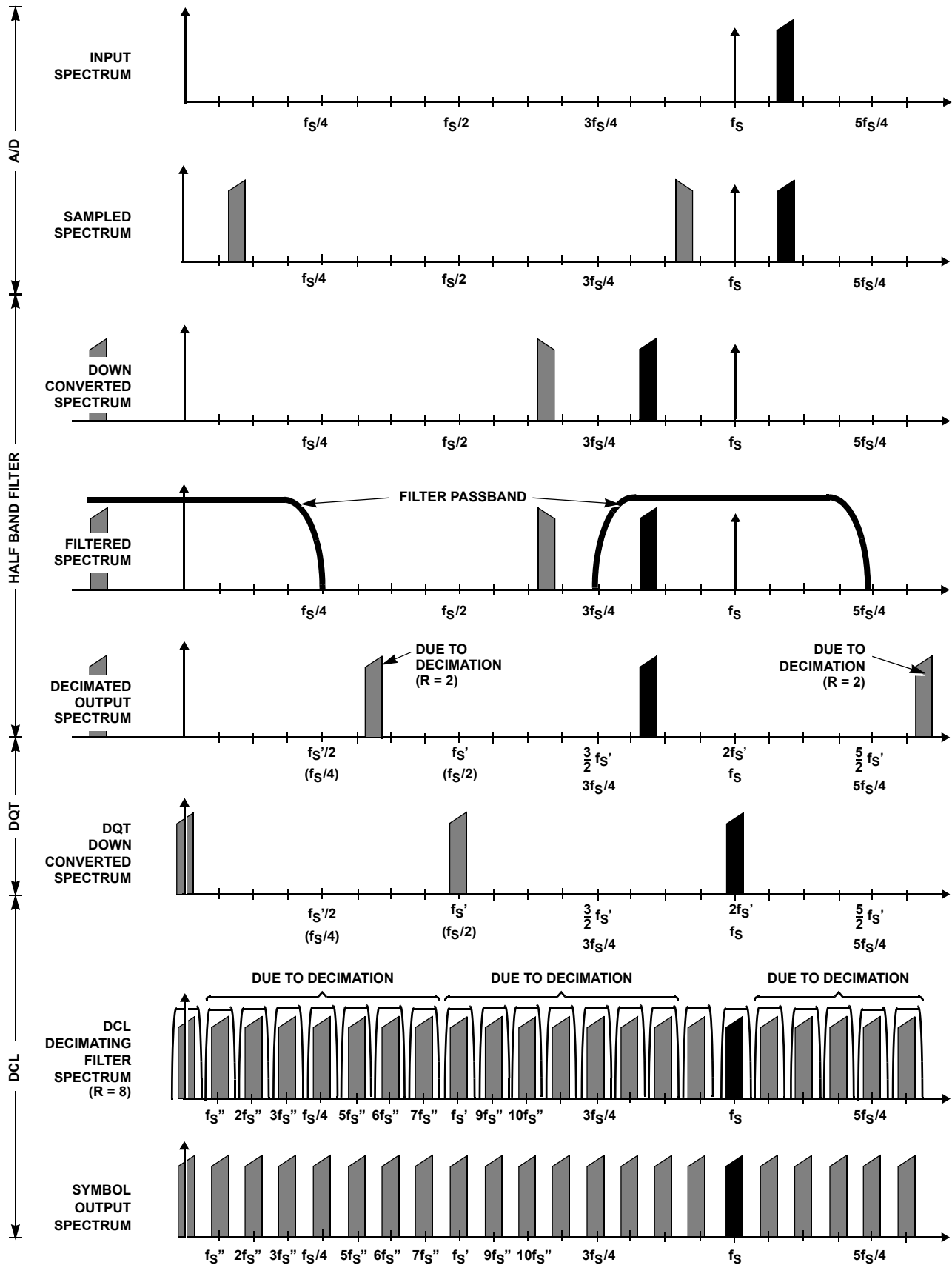
NOTE: $f_S = 2f_S' = 16f_S''$

FIGURE 3. HIGH RATE RECEIVER SPECTRAL DEVELOPMENT

Matched Baseband Filter Requirements

The final receiver design consideration is the construction of a matched baseband filter for the received signal. The DQT/DCL chipset offers two filters integral to the chip: 1) Integrate and Dump and 2) Square Root of Raised Cosine α = 0.4. If one of these filters meets your system performance requirements, then no further design is required.

If your application requires a different filter, the HSP43168 or the HSP43124 can be inserted between the DQT and the DCL. The serial I/O filter (HSP43124) is limited to CLK = (45MHz/bit width). The Dual FIR filter (HSP43168) is limited to CLK = 45MHz. These parts may become the limiting factor for the maximum clock speed. This translates to an A/D sample rate at 90MHz, an A/D dual demultiplexed data output rate of 45MHz, a Halfband Filter dual data Output Rate of 45MHz, and a symbol rate of 22.5MHz. In general, filtering requirements may demand that greater than eight taps be used in the filter, and two HSP43168 chips may be required (one for I, one for Q) for adequate shaping.

Summary

Figure 1 outlines the implementation of the high symbol rate receiver. The solution assumes the need for an application specific matched filter, limiting the symbol rate to 22.5MHz. Key elements of the design are: the anti-alias filter, the quadrature output A/D converter, the dual input decimating Halfband Filter, the Digital Quadrature Tuner and the Digital Costas loop. The design uses the level detection feature of the HSP50110 to drive a Voltage Controlled Attenuator to keep the level at the converter input at an optimum value.

For information relative to setting the internal PLL parameters in the DQT/DCL chipset, refer to the HSP50110/210 EVAL Users Manual.

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